2escription

SP002GBSTU133S01 is 204Pin Double Data Rate 3 (DDR3) Synchronous DRAM Small Outline Dual In-Line Memory Module, organized as one rank of 256Mx64 (2GB) high-speed memory array.

Modules use sixteen 128Mx8 (1Gb) 78-ball BGA packaged devices.

This DIMM are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. DDR3 SDRAM DIMM provide a high-performance, flexible 8-byte interface in a space-saving footprint.

The DIMM is intended for use in applications operating of 667MHz clock speeds and achieves high-speed data transfer rates of 1333Mbps. Prior to any access operation, the device CAS latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0~BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of SPD data are programmed during module assembly. The remaining 128 bytes are available for use by the customer.

Features

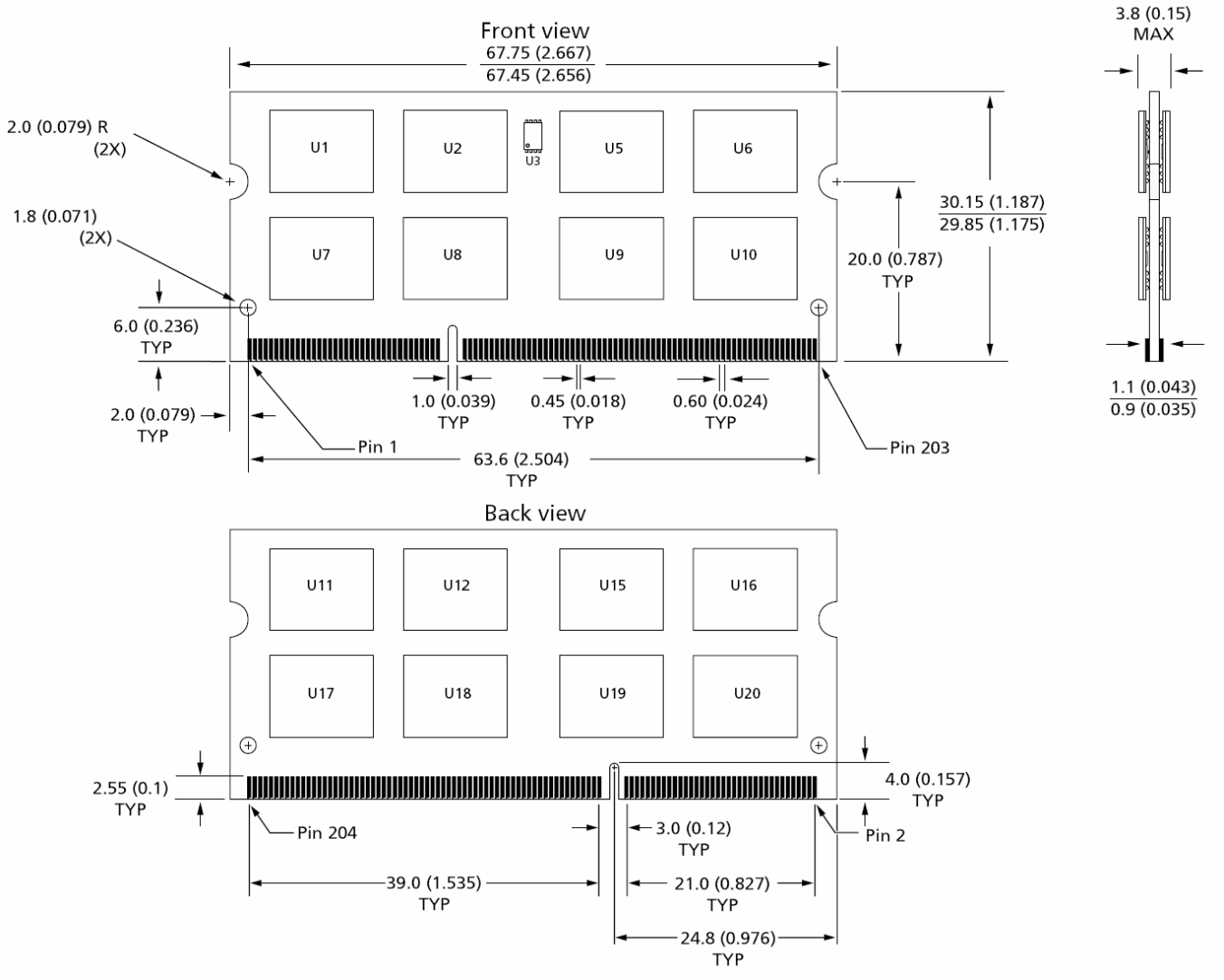
- DDR3 functionality and operations supported as per the component data sheet
- 204pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC3-10600
- 2GB (256 Meg x 64)
- VDD = 1.5V ±0.075V (SSTL_15)
- VDDSPD = +3.0V to +3.6V
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Single rank
- On-board I2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Pb-free
- Fly-by topology
- Terminated control, command, and address bus

Module Specification

Item	Specification
Capacity	2G Byte
Physical Rank(s)	2 Ranks
Module Organization	256M x 64bit
Module Type	SODIMM
Speed Grade	PC3-10600 / (DDR3 1333)
Voltage Interface	SSTL_15
Power Supply Voltage	1.5V ± 0.075V
Burst Lengths	8
DRAM Organization	DDR3 SDRAM 128M x 8bit
PCB Layer	8Layers
Contact Tab	204 pin GOLD Flash Plating
Serial PD	Support

Simplified Mechanical Drawing

X64 DIMM, populated as two physical ranks of x8 DDR3 SDRAMs



Note 1: All dimensions are typical unless otherwise stated. (Millimeters)

Note 2: The dimensional diagram is for reference only.

Pin Assignments

204-Pin DDR3 SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	53	DQ19	105	VDD	157	DQ42
3	VSS	55	VSS	107	A10	159	DQ43
5	DQ0	57	DQ24	109	BA0	161	VSS
7	DQ1	59	DQ25	111	VDD	163	DQ48
9	VSS	61	VSS	113	WE#	165	DQ49
11	DM0	63	DM3	115	CAS#	167	VSS
13	VSS	65	VSS	117	VDD	169	DQS6#
15	DQ2	67	DQ26	119	A13	171	DQS6
17	DQ3	69	DQ27	121	CS1#	173	VSS
19	VSS	71	VSS	123	VDD	175	DQ50
21	DQ8	73	CKE0	125	NC	177	DQ51
23	DQ9	75	VDD	127	VSS	179	VSS
25	VSS	77	NC	129	DQ32	181	DQ56
27	DQS1#	79	BA2	131	DQ33	183	DQ57
29	DQS1	81	VDD	133	VSS	185	VSS
31	VSS	83	A12	135	DQS4#	187	DM7
33	DQ10	85	A9	137	DQS4	189	VSS
35	DQ11	87	VDD	139	VSS	191	DQ58
37	VSS	89	A8	141	DQ34	193	DQ59
39	DQ16	91	A5	143	DQ35	195	VSS
41	DQ17	93	VDD	145	VSS	197	SA0
43	VSS	95	A3	147	DQ40	199	VDDSPD
45	DQS2#	97	A1	149	DQ41	201	SA1
47	DQS2	99	VDD	151	VSS	203	VTT
49	VSS	101	CK0	153	DM5	–	–
51	DQ18	103	CK0#	155	VSS	–	–

204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	VSS	54	VSS	106	VDD	158	DQ46
4	DQ4	56	DQ28	108	BA1	160	DQ47
6	DQ5	58	DQ29	110	RAS#	162	VSS
8	VSS	60	VSS	112	VDD	164	DQ52
10	DQS0#	62	DQS3#	114	CS0#	166	DQ53
12	DQS0	64	DQS3	116	ODT0	168	VSS
14	VSS	66	VSS	118	VDD	170	DM6
16	DQ6	68	DQ30	120	ODT1	172	VSS
18	DQ7	70	DQ31	122	NC	174	DQ54
20	VSS	72	VSS	124	VDD	176	DQ55
22	DQ12	74	CKE1	126	VREFCA	178	VSS
24	DQ13	76	VDD	128	SS	180	DQ60
26	VSS	78	NC	130	DQ36	182	DQ61
28	DM1	80	NC/A14	132	DQ37	184	VSS
30	RESET#	82	VDD	134	VSS	186	DQS7#
32	VSS	84	A11	136	DM4	188	DQS7
34	DQ14	86	A7	138	VSS	190	VSS
36	DQ15	88	VDD	140	DQ38	192	DQ62
38	VSS	90	A6	142	DQ39	194	DQ63
40	DQ20	92	A4	144	VSS	196	VSS
42	DQ21	94	VDD	146	DQ44	198	EVENT#
44	VSS	96	A2	148	DQ45	200	SDA
46	DM2	98	A0	150	VSS	202	SCL
48	VSS	100	VDD	152	DQS5#	204	VTT
50	DQ22	102	CK1	154	DQS5	–	–
52	DQ23	104	CK1#	156	VSS	–	–

Pin Description

Symbol	Type	Description
A[14:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as "BL on-the-fly" during CAS commands. The address inputs also provide the op-code during the mode register command set. A[12:0] address the 1Gb DDR3 devices. A[13:0] address the 1Gb DDR3 devices. A[14:0] address the 2Gb DDR3 devices.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command. BA[2:0] are used as part of the parity calculation.
CK[1:0], CK#[1:0]	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE[1:0]	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DM[7:0]	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of the DQS. Although the DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
ODT[1:0]	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DRAM. When enabled in normal operation, ODT is applied only to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW CMOS input referenced to Vss. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × Vdd and DC LOW ≤ 0.2 × Vdd.
CS#[1:0]	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Serial address inputs:** These pins are used to configure the temperature sensor/SPD EEPROM address range on the I2C bus.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[8:0], DQS#[8:0]	I/O	**Data strobe:** DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. DQS# is used only when the differential data strobe mode is enabled via the LOAD MODE command.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** SCL is used to synchronize communication to and from the temperature sensor/SPD EEPROM.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the module on the I2C bus.
Vdd	Supply	**Power supply:** 1.5V ±0.075V. The component Vdd and Vddq are connected to the module Vdd.
Vddspd	Supply	**Temperature sensor/SPD EEPROM power supply:** +3.0V to +3.6V.
Vrefca	Supply	**Reference voltage:** Control, command, and address (Vdd/2).
Vrefdq	Supply	**Reference voltage:** DQ, DM (Vdd/2).
Vss	Supply	Ground.
Vtt	Supply	**Termination voltage:** Used for control, command, and address (Vdd/2).
NC	–	**No connect:** These pins are not connected on the module.
NU	–	**Not used:** These pins are not used in specific module configuration/operations.