## 1. Features

- 240-pin, unbuffered dual in-line memory module
- Fast data transfer rates: PC3-10600
- VDD = VDDQ = +1.5V ±0.075V
- VDDSPD = +3.0V to +3.6V
- Interface: SSTL_15
- Programmable CAS Latency: 6, 7,8,9
- Reset pin for improved system stability
- 8 internal device banks for concurrent operation
- Fixed burst length of 8 (BL8) and burst chop of 4 (BC4) via the mode register
- Adjustable data-output drive strength
- Serial presence-detect (SPD) EEPROM
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- ZQ calibration for DQ drive and ODT
- Fly-by topology
- Terminated command, address, and control bus
- Refresh cycles Average refresh period

  7.8µs at 0℃ ≤ TC ≤ +85℃

  3.9µs at +85℃ < TC ≤ +95℃
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- On-Die-Termination (ODT) for better signal quality

  Synchronous ODT

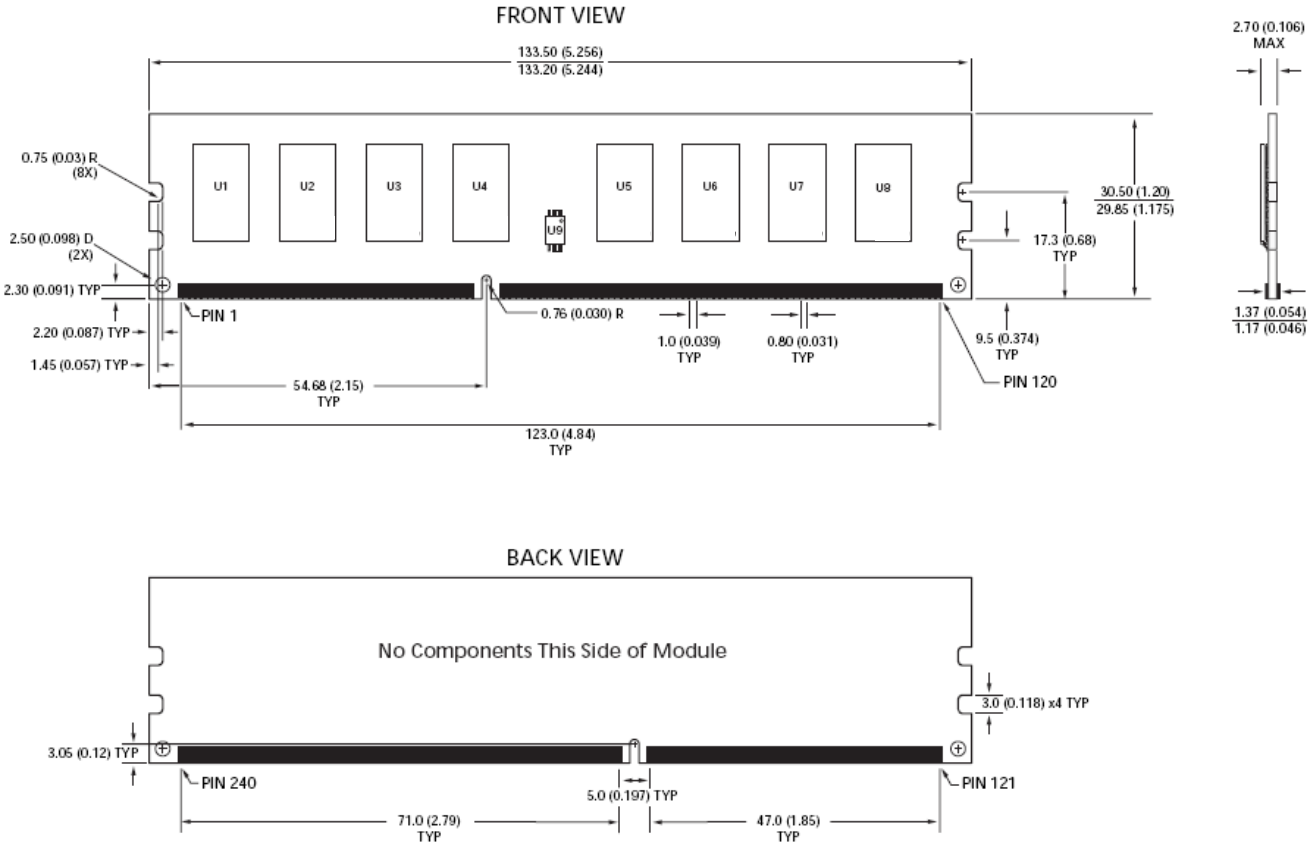
  Dynamic ODT

  Asynchronous ODT

## 2. Module Specification

| Item | Specification |
|---|---|
| Capacity | 1024MByte |
| Physical Bank(s) | 1 |
| Module Organization | 128M x 64bit |
| Module Type | Unbuffered Non ECC |
| Speed Grade | PC3-10600 / (DDR3 1333) |
| Voltage Interface | SSTL_15 |
| Power Supply Voltage | 1.5V ± 0.075V |
| Burst Lengths | 4 or 8 |
| DRAM Organization | 128M x 8bit DDR3 SDRAM |
| PCB Layer | 6Layers |
| Contact Tab | 240 pin GOLD Flash Plating |
| Serial PD | Support |

## 3. Simplified Mechanical Drawing with Keying Positions




***Notes*** **：** 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

2.The dimensional diagram is for reference only.

## 4. Pinouts

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VREFDQ | 31 | DQ25 | 61 | A2 | 91 | DQ41 | 121 | VSS | 151 | VSS | 181 | A1 | 211 | VSS |
| 2 | VSS | 32 | VSS | 62 | VDD | 92 | VSS | 122 | DQ4 | 152 | DM3 | 182 | VDD | 212 | DM5 |
| 3 | DQ0 | 33 | DQS3# | 63 | NC | 93 | DQS5# | 123 | DQ5 | 153 | NC | 183 | VDD | 213 | NC |
| 4 | DQ1 | 34 | DQS3 | 64 | NC | 94 | DQS5 | 124 | VSS | 154 | VSS | 184 | CK0 | 214 | VSS |
| 5 | VSS | 35 | VSS | 65 | VDD | 95 | VSS | 125 | DM0 | 155 | DQ30 | 185 | CK0# | 215 | DQ46 |
| 6 | DQS0# | 36 | DQ26 | 66 | VDD | 96 | DQ42 | 126 | NC | 156 | DQ31 | 186 | VDD | 216 | DQ47 |
| 7 | DQS0 | 37 | DQ27 | 67 | VREFCA | 97 | DQ43 | 127 | VSS | 157 | VSS | 187 | NC | 217 | VSS |
| 8 | VSS | 38 | VSS | 68 | NC | 98 | VSS | 128 | DQ6 | 158 | NC | 188 | A0 | 218 | DQ52 |
| 9 | DQ2 | 39 | NC | 69 | VDD | 99 | DQ48 | 129 | DQ7 | 159 | NC | 189 | VDD | 219 | DQ53 |
| 10 | DQ3 | 40 | NC | 70 | A10 | 100 | DQ49 | 130 | VSS | 160 | VSS | 190 | BA1 | 220 | VSS |
| 11 | VSS | 41 | VSS | 71 | BA0 | 101 | VSS | 131 | DQ12 | 161 | NC | 191 | VDD | 221 | DM6 |
| 12 | DQ8 | 42 | NC | 72 | VDD | 102 | DQS6# | 132 | DQ13 | 162 | NC | 192 | RAS# | 222 | NC |
| 13 | DQ9 | 43 | NC | 73 | WE# | 103 | DQS6 | 133 | VSS | 163 | VSS | 193 | S0# | 223 | VSS |
| 14 | VSS | 44 | VSS | 74 | CAS# | 104 | VSS | 134 | DM1 | 164 | NC | 194 | VDD | 224 | DQ54 |
| 15 | DQS1# | 45 | NC | 75 | VDD | 105 | DQ50 | 135 | NC | 165 | NC | 195 | ODT0 | 225 | DQ55 |
| 16 | DQS1 | 46 | NC | 76 | NC | 106 | DQ51 | 136 | VSS | 166 | VSS | 196 | A13 | 226 | VSS |
| 17 | VSS | 47 | VSS | 77 | NC | 107 | VSS | 137 | DQ14 | 167 | NC | 197 | VDD | 227 | DQ60 |
| 18 | DQ10 | 48 | NC | 78 | VDD | 108 | DQ56 | 138 | DQ15 | 168 | RESET# | 198 | NC | 228 | DQ61 |
| 19 | DQ11 | 49 | NC | 79 | NC | 109 | DQ57 | 139 | VSS | 169 | NC | 199 | VSS | 229 | VSS |
| 20 | VSS | 50 | CKE0 | 80 | VSS | 110 | VSS | 140 | DQ20 | 170 | VDD | 200 | DQ36 | 230 | DM7 |
| 21 | DQ16 | 51 | VDD | 81 | DQ32 | 111 | DQS7# | 141 | DQ21 | 171 | NC | 201 | DQ37 | 231 | NC |
| 22 | DQ17 | 52 | BA2 | 82 | DQ33 | 112 | DQS7 | 142 | VSS | 172 | NC | 202 | VSS | 232 | VSS |
| 23 | VSS | 53 | NC | 83 | VSS | 113 | VSS | 143 | DM2 | 173 | VDD | 203 | DM4 | 233 | DQ62 |
| 24 | DQS2# | 54 | VDD | 84 | DQS4# | 114 | DQ58 | 144 | NC | 174 | A12 | 204 | NC | 234 | DQ63 |
| 25 | DQS2 | 55 | A11 | 85 | DQS4 | 115 | DQ59 | 145 | VSS | 175 | A9 | 205 | VSS | 235 | VSS |
| 26 | VSS | 56 | A7 | 86 | VSS | 116 | VSS | 146 | DQ22 | 176 | VDD | 206 | DQ38 | 236 | VDDSPD |
| 27 | DQ18 | 57 | VDD | 87 | DQ34 | 117 | SA0 | 147 | DQ23 | 177 | A8 | 207 | DQ39 | 237 | SA1 |
| 28 | DQ19 | 58 | A5 | 88 | DQ35 | 118 | SCL | 148 | VSS | 178 | A6 | 208 | VSS | 238 | SDA |
| 29 | VSS | 59 | A4 | 89 | VSS | 119 | SA2 | 149 | DQ28 | 179 | VDD | 209 | DQ44 | 239 | VSS |
| 30 | DQ24 | 60 | VDD | 90 | DQ40 | 120 | VTT | 150 | DQ29 | 180 | A3 | 210 | DQ45 | 240 | VTT |

***Note*** **:** Pin 172 is NC for 1GB and A14 for 2GB

# 5. Pin Description

| SYMBOL | TYPE | DESCRIPTION |
|---|---|---|
| CK0, CK0# | Input | **Clock:** CK0 and CK0# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#. CK1, CK1# are terminated. |
| CKE0 | Input | **Clock Enable:** CKE (registered HIGH) activates and CKE(registered LOW) deactivates clocking circuitry on the DDR3 SDRAM |
| S0# | Input | **Chip Select:** S# enables (registered LOW) and disables (registered High) the command decoder. With both input High, all outputs of the register(s) are disabled except for CKE and ODT. CKE, ODT and chip select remain in previous state when both outputs are high. |
| ODT0 | Input | **On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, and DQS#. The ODT input will be ignored if disabled via the LOAD MODE command. |
| RAS#, #CAS, WE# | Input | **Command Inputs:** RAS#, CAS# and WE# (along with S#) define the command being entered. |
| DM0-DM7 | Input | **Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a Write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that DQ and DQS pin. |
| BA0 - BA2 | Input | **Bank Address Inputs:** BA0-BA2 define to which device bank an Active, Read, Write or Precharge command is being applied. BA0-BA2 define which mode register, including MR, EMR, EMR(2), EMR(3), is loaded during the LOAD MODE command. |
| A0 - A14 | Input | **Address Inputs:** Provided the row address for Active commands and the column address and auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge, applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is sampled during READ and WRITE commands to determine if burst chop(on-the-fly) will be performed. The address inputs also provide the op-code during Mode Register Set command set. A0-A13(1GB) A0-A14(2GB) |
| DQ0-DQ63 | Input/Output | **Data bit Input/ Output:** Bi-directional data bus. |
| DQS0-DQS7<br>DQS0#-DQS7# | Input/Output | **Data Strobe:** output with read data, input with write data for source-synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. |
| RESET# | Input | **Reset:** Set DRAM to known state |
| NC | | **No Connect:** These pins should be left unconnected. |
| $V_{DD}$ | Supply | **Power supply:** 1.5V±0.075V. |
| $V_{REF}$DQ | Supply | **Reference voltage:** DQ, DM, VDD/2 |
| $V_{REF}$CA | Supply | **Reference voltage:** Command, Address, and control, VDD/2 |
| SDA | Input/Output | **Serial presence-detect data :** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module. |
| SCL | Input | **Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module. |
| $V_{DD}$SPD | Supply | **Serial EEPROM positive power supply:** 3.0V to 3.6V. |
| SA0-SA2 | Input | **Presence-detect address inputs:** These pins are used to configure the SPD EEPROM address range. |
| VSS | Supply | **Ground.** |
| VTT | Supply | **Termination voltage:** Used for address, command, control, and clock net. VDD/2 |