Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 240pin, Registered Dual In-line Memory Module (RDIMM)
- Supports ECC error detection and correction
- Fast data transfer rates: PC3-8500, PC3-10600, PC3-12800
- Single Rank, Dual ranks or Quad Ranks
- 1GB(128 Meg x 72), 2GB (256 Meg x 72), 4GB (512 Meg x 72), 8GB(1024Meg x 72)
- $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- V_{DD}SPD = 3.0V to 3.6V
- Reset pin for improved system stability
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Adjustable data-output drive strength
- Fly-by topology
- Terminated control, command, and address bus
- Serial presence-detect (SPD) EEPROM
- Gold edge contacts
- Pb-free

Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing (tCL-tRCD-tRP)
SP001GBRTE106S01	1GB (128Mx72) 128Mx8 1Rank	PC3-8500	DDR3-1066	7-7-7
SP001GBRTE133S01		PC3-10600	DDR3-1333	9-9-9
SP002GBRTE106S01	2GB (256Mx64) 128Mx8 2Ranks	PC3-8500	DDR3-1066	7-7-7
SP002GBRTE133S01		PC3-10600	DDR3-1333	9-9-9
SP004GBRTE133S01	4GB (512Mx64) 128Mx8 4Ranks	PC3-10600	DDR3-1333	9-9-9
SP004GBRTE133U01	4GB (512Mx64) 256Mx4 2Ranks	PC3-10600	DDR3-1333	9-9-9
SP004GBRTE133V01	4GB (512Mx64) 256Mx8 2Ranks	PC3-10600	DDR3-1333	9-9-9
SP008GBRTE133M0A	8GB (512Mx64) 512Mx4 2Ranks	PC3-10600	DDR3-1333	9-9-9

Note:

1. This document supports all RTE Series DDR3 240Pin RDIMM products.
2. Some item was being EOL in this list, Please contact with our sales Dep.
3. All part numbers end with a double-digit code is for customize use only.
   Example: SP001GBRTE133S01-XX

Pin Assignments

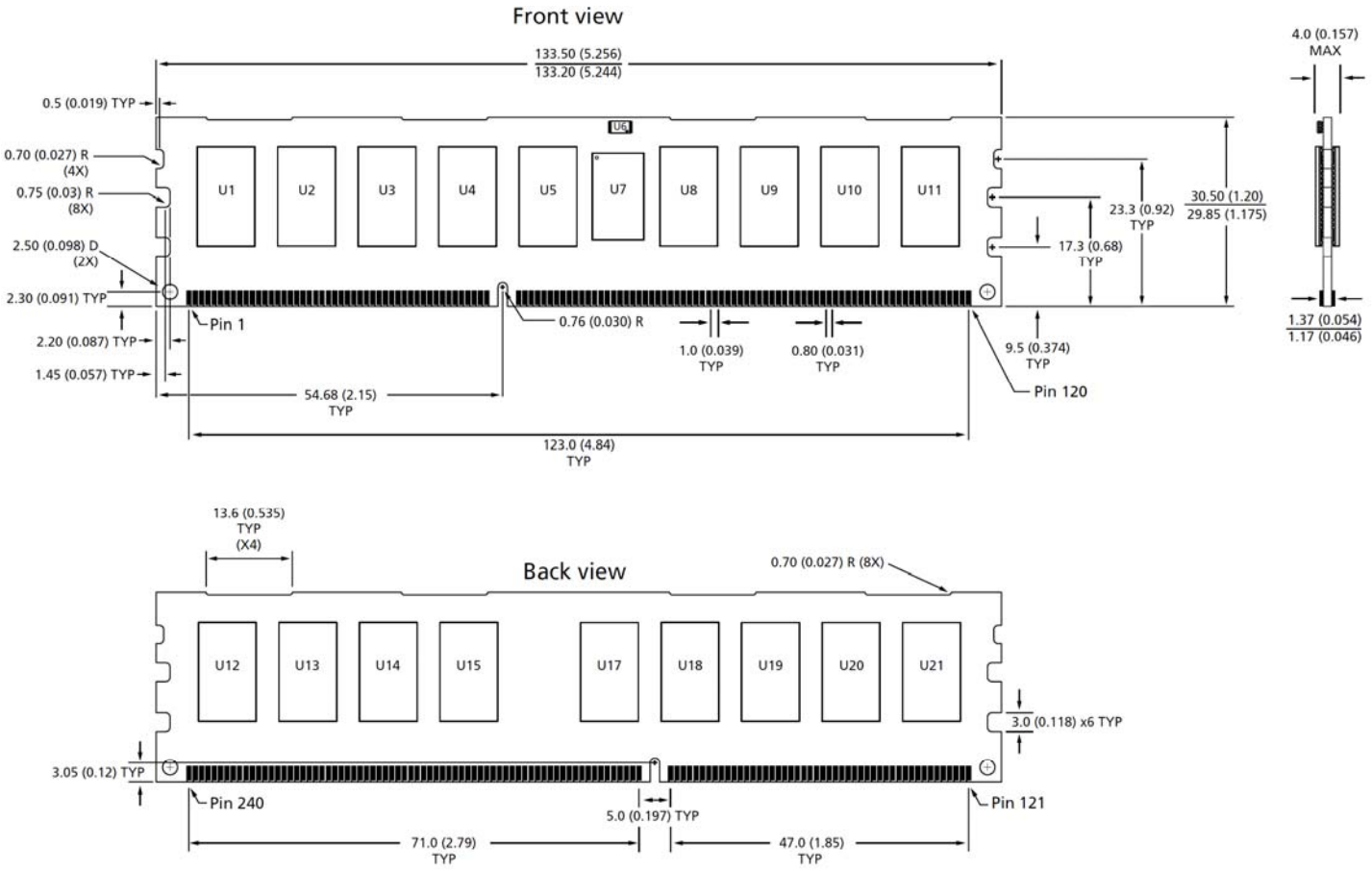
240-Pin DDR3 RDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	$V_{REF}DQ$	31	DQ25	61	A2	91	DQ41
2	V_{SS}	32	V_{SS}	62	V_{DD}	2	V_{SS}
3	DQ0	33	DQS3#	63	NC	93	DQS5#
4	DQ1	34	DQS3	64	NC	94	DQS5
5	V_{SS}	35	V_{SS}	65	V_{DD}	95	V_{SS}
6	DQS0#	36	DQ26	66	V_{DD}	96	DQ42
7	DQS0	37	DQ27	67	$V_{REF}CA$	97	DQ43
8	V_{SS}	38	V_{SS}	68	Par_In	98	V_{SS}
9	DQ2	39	CB0	69	V_{DD}	99	DQ48
10	DQ3	40	CB1	70	A10	100	DQ49
11	V_{SS}	41	V_{SS}	71	BA0	101	V_{SS}
12	DQ8	42	DQS8#	72	V_{DD}	102	DQS6#
13	DQ9	43	DQS8	73	WE#	103	DQS6
14	V_{SS}	44	V_{SS}	74	CAS#	104	V_{SS}
15	DQS1#	45	CB2	75	V_{DD}	105	DQ50
16	DQS1	46	CB3	76	S1#	106	DQ51
17	V_{SS}	47	V_{SS}	77	ODT1	107	V_{SS}
18	DQ10	48	V_{TT}	78	V_{DD}	108	DQ56
19	DQ11	49	V_{TT}	79	NC	109	DQ57
20	V_{SS}	50	CKE0	80	V_{SS}	110	V_{SS}
21	DQ16	51	V_{DD}	81	DQ32	111	DQS7#
22	DQ17	52	BA2	82	DQ33	112	DQS7
23	V_{SS}	53	Err_Out#	83	V_{SS}	113	V_{SS}
24	DQS2#	54	V_{DD}	84	DQS4#	114	DQ58
25	DQS2	55	A11	85	DQS4	115	DQ59
26	V_{SS}	56	A7	86	V_{SS}	116	V_{SS}
27	DQ18	57	V_{DD}	87	DQ34	117	SA0
28	DQ19	58	A5	88	DQ35	118	SCL
29	V_{SS}	59	A4	89	V_{SS}	119	SA2
30	DQ24	60	V_{DD}	90	DQ40	120	Vtt

240-Pin DDR3 RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	V_{SS}	151	V_{SS}	181	A1	211	V_{SS}
122	DQ4	152	DM3/ DQS12/ TDQS12	182	V_{DD}	212	DM5/ DQS14/ TDQS14
123	DQ5	153	NU/ DQS12#/ TDQS12#	183	V_{DD}	213	NU/ DQS14#/ TDQS14#
124	V_{SS}	154	V_{SS}	184	CK0	214	V_{SS}
125	DM0/ DQS9/ TDQS9	155	DQ30	185	CK0#	215	DQ46
126	NU/ DQS9#/ TDQS9#	156	DQ31	186	V_{DD}	216	DQ47
127	V_{SS}	157	V_{SS}	187	EVENT#	217	VSS
128	DQ6	158	CB4	188	A0	218	DQ52
129	DQ7	159	CB5	189	V_{DD}	219	DQ53
130	V_{SS}	160	V_{SS}	190	BA1	220	V_{SS}
131	DQ12	161	DM8/ DQS17 / TDQS17	191	V_{DD}	221	DM6/ DQS15/ TDQS15
132	DQ13	162	NU/ DQS17#/ TDQS17#	192	RAS#	222	NU/ DQS15#/ TDQS15#
133	V_{SS}	163	V_{SS}	193	S0#	223	V_{SS}
134	DM1/ DQS10/ TDQS10	164	CB6	194	V_{DD}	224	DQ54
135	NU/ DQS10#/ TDQS10#	165	CB7	195	ODT0	225	DQ55
136	V_{SS}	166	V_{SS}	196	A13	226	V_{SS}
137	DQ14	167	NC	197	V_{DD}	227	DQ60
138	DQ15	168	RESET#	198	NC	228	DQ61
139	V_{SS}	169	CKE1	199	V_{SS}	229	V_{SS}
140	DQ20	170	V_{DD}	200	DQ36	230	DM7/ DQS16/ TDQS16
141	DQ21	171	A15	201	DQ37	231	NU/ DQS16# TDQS16#
142	V_{SS}	172	A14	202	V_{SS}	232	V_{SS}
143	DM2/ DQS11/ TDQS11	173	V_{DD}	203	DM4/ DQS13/ TDQS13	233	DQ62
144	NU/ DQS11#/ TDQS11#	174	A12	204	NU/ DQS13# TDQS13#	234	DQ63
145	V_{SS}	175	A9	205	V_{SS}	235	V_{SS}
146	DQ22	176	V_{DD}	206	DQ38	236	$V_{DD}SPD$
147	DQ23	177	A8	207	DQ39	237	SA1
148	V_{SS}	178	A6	208	V_{SS}	238	SDA
149	DQ28	179	V_{DD}	209	DQ44	239	V_{SS}
150	DQ29	180	A3	210	DQ45	240	V_{TT}

Pin Description

Symbol	Type	Description
A[15:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as “BL on-the-fly” during CAS commands. The address inputs also provide the op-code during the mode register command set. A[13:0] address the 1Gb DDR3 devices. A[15:14] are needed to calculate parity on the command/address bus.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command. BA[2:0] are used as part of the parity calculation.
CK0, CK0#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE[1:0]	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DM[8:0] (TDQS[17:9], TDQS#[17:9])	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of the DQS. Although the DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins. When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance, otherwise the TDQS# pins are no function.
ODT[1:0]	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DRAM. When enabled in normal operation, ODT is applied only to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for the address, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 ×V_{DD} and DC LOW ≤ 0.2 × V_{DD}.
S#[3:0]	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Serial address inputs:** These pins are used to configure the temperature sensor/SPD EEPROM address range on the I2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** SCL is used to synchronize communication to and from the temperature sensor/SPD EEPROM.
CB[7:0]	I/O	**Check bits:** Data used for ECC.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[8:0], DQS#[8:0]	I/O	**Data strobe:** DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. DQS# is used only when the differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the module on the I2C bus.
Err_Out#	Output (open-drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open-drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DD}SPD	Supply	**Temperature sensor/SPD EEPROM power supply:** +3.0V to +3.6V.
V_{REF}CA	Supply	**Reference voltage:** Control, command, and address (V_{DD} /2).
V_{REF}DQ	Supply	**Reference voltage:** DQ, DM (V_{DD} /2).
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address (V_{DD} /2).
NC	–	**No connect:** These pins are not connected on the module.
NU	–	**Not used:** These pins are not used in specific module configuration/operations.

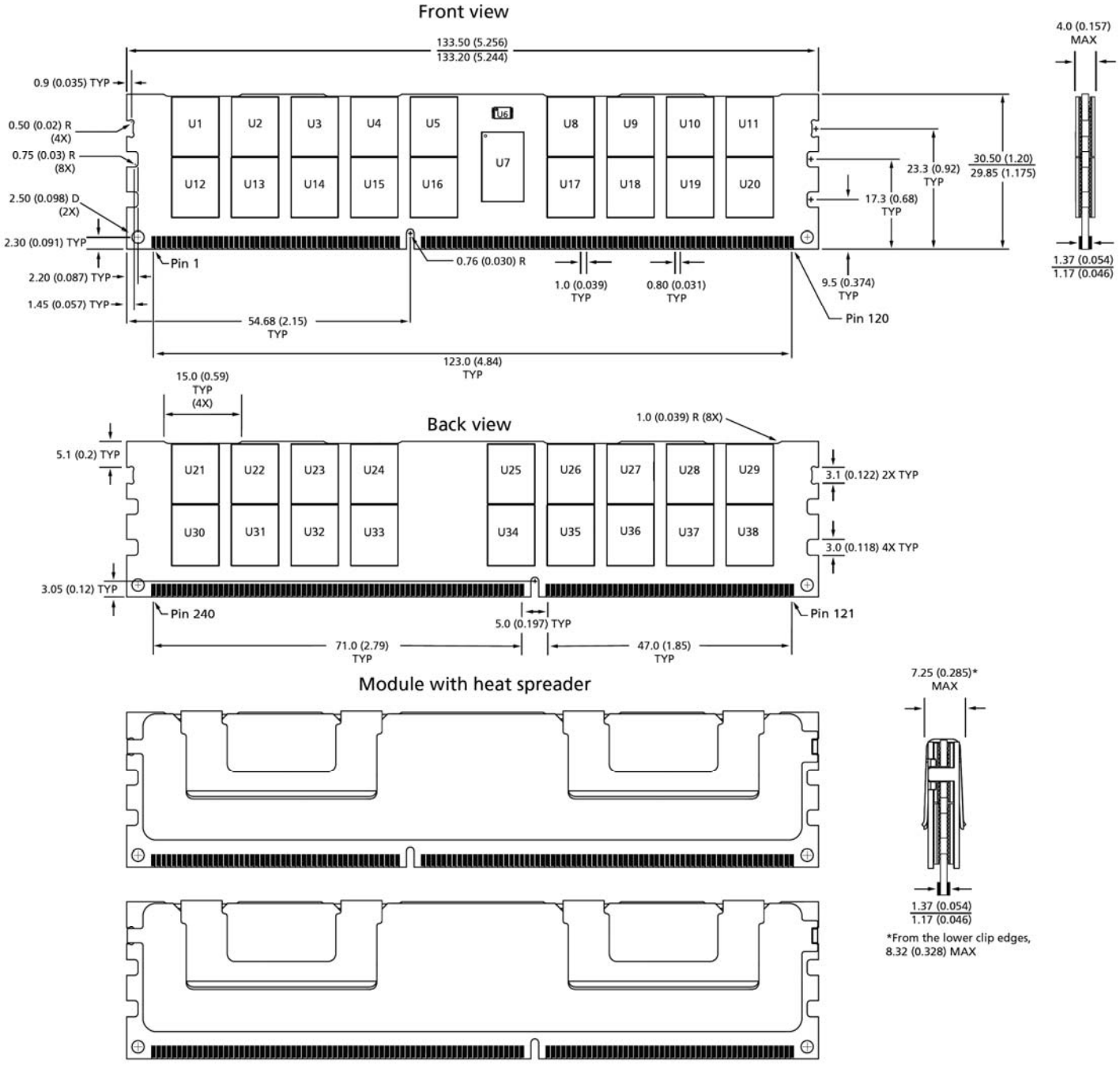
Simplified Mechanical Drawing(x4 1Rank)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

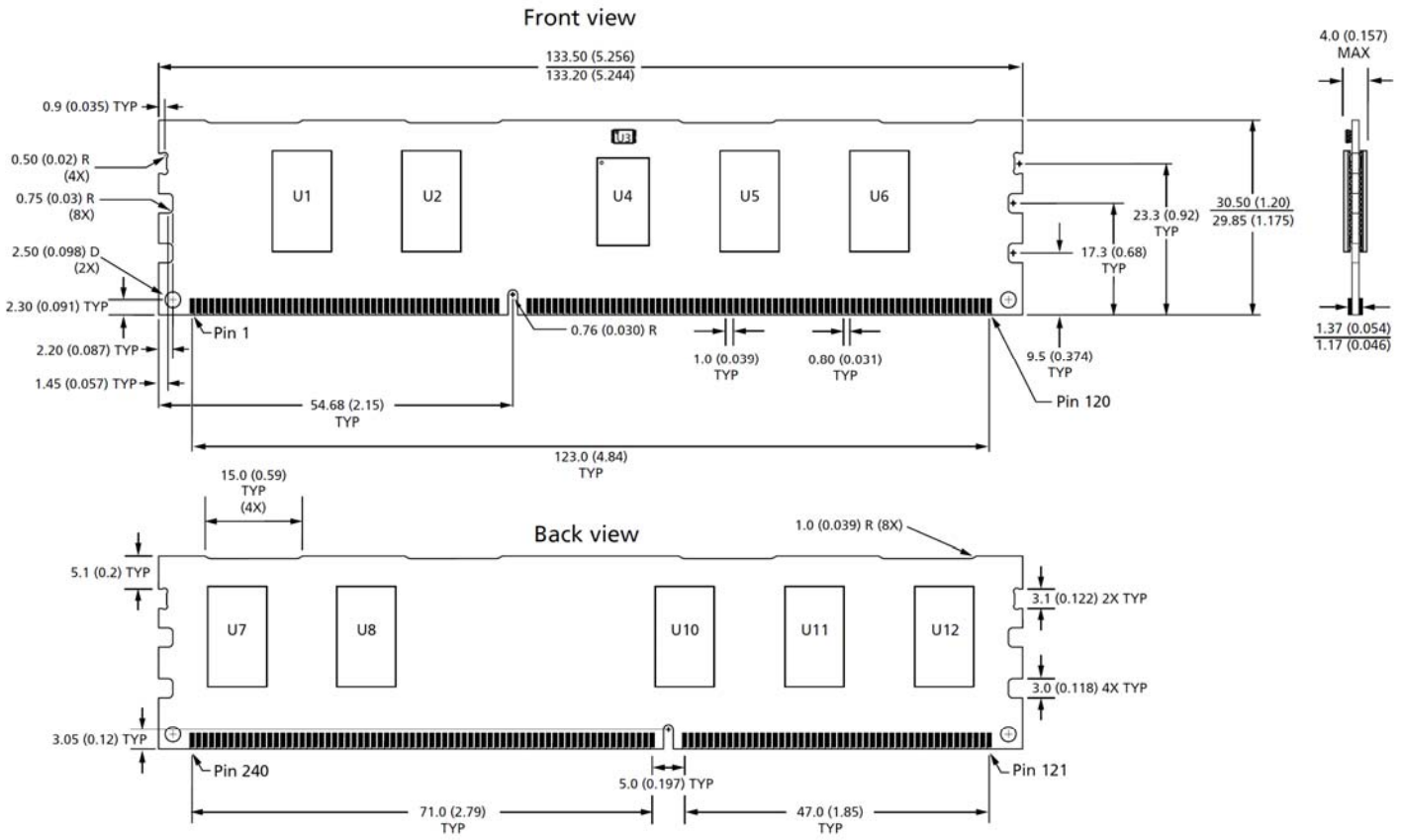
Simplified Mechanical Drawing(x4 2Ranks)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

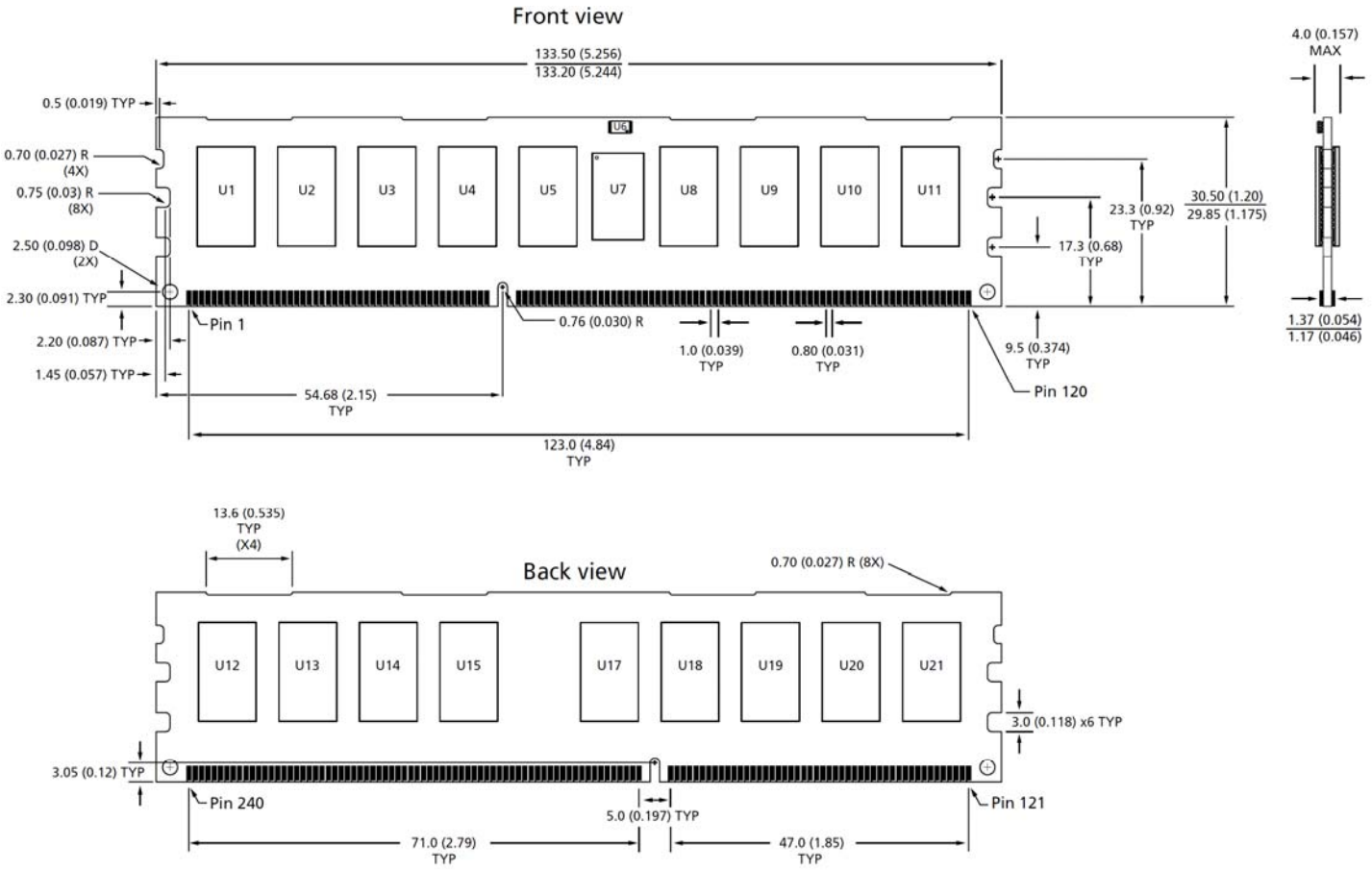
Simplified Mechanical Drawing(x8 1Rank)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

Simplified Mechanical Drawing(x8 2Ranks)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.