Features

• DDR3 functionality and operations supported as defined in the component data sheet
• 240-pin, ECC Unbuffered Dual In-line Memory Module (ECCDIMM)
• Fast data transfer rates: PC3-8500, PC3-10600
• 1GB(128 Meg x 72), 2GB (256 Meg x 72), 4GB (512Meg x 72)
• V_{DD} = V_{DDQ} = 1.5V ±0.075V
• V_{DDSPD} = 3.0V to 3.6V
• Supports ECC error detection and correction
• Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
• Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
• Adjustable data-output drive strength
• Serial presence-detect (SPD) EEPROM
• Gold edge contacts
• Pb-free
• Fly-by topology
• Terminated control, command, and address bus

Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing (tCL-tRCD-tRP)
SP001GBLTE106S01	1GB (128Mx64) 128Mx8 1Rank	PC3-8500	DDR3-1066	7-7-7
SP001GBLTE133S01		PC3-10600	DDR3-1333	9-9-9
SP002GBLTE106S01	2GB (256Mx64) 128Mx8 2Ranks	PC3-8500	DDR3-1066	7-7-7
SP002GBLTE133S01		PC3-10600	DDR3-1333	9-9-9
SP004GBLTE133V01	2GB (256Mx64) 256Mx8 1Rank	PC3-10600	DDR3-1333	9-9-9

Note:

This document supports all LTE Series DDR3 240Pin ECCDIMM products.

Some item was be EOL in this list, Please contact with our sales Dep.

Pin Assignments

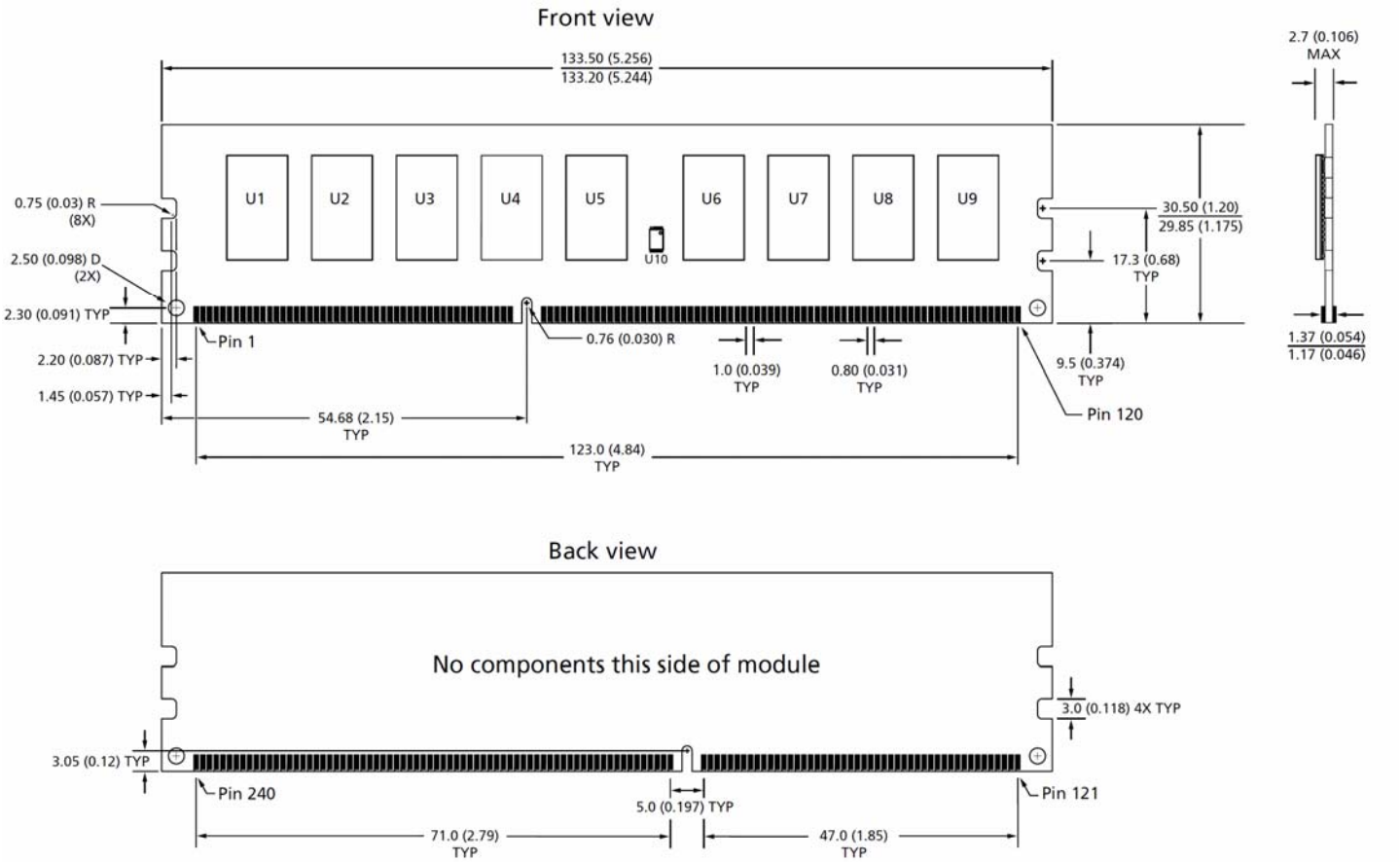
240-Pin DDR3 ECC DIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vrefdq	31	DQ25	61	A2	91	DQ41
2	Vss	32	Vss	62	Vdd	92	Vss
3	DQ0	33	DQS3#	63	CK1/NC	93	DQS5#
4	DQ1	34	DQS3	64	CK1#/NC	94	DQS5
5	Vss	35	Vss	65	Vdd	95	Vss
6	DQS0#	36	DQ26	66	Vdd	96	DQ42
7	DQS0	37	DQ27	67	Vrefca	97	DQ43
8	Vss	38	Vss	68	NC	98	Vss
9	DQ2	39	CB0	69	Vdd	99	DQ48
10	DQ3	40	CB1	70	A10	100	DQ49
11	Vss	41	Vss	71	BA0	101	Vss
12	DQ8	42	DQS8#	72	Vdd	102	DQS6#
13	DQ9	43	DQS8	73	WE#	103	DQS6
14	Vss	44	Vss	74	CAS#	104	Vss
15	DQS1#	45	CB2	75	Vdd	105	DQ50
16	DQS1	46	CB3	76	S1#	106	DQ51
17	Vss	47	Vss	77	ODT1	107	Vss
18	DQ10	48	NC	78	Vdd	108	DQ56
19	DQ11	49	NC	79	NC	109	DQ57
20	Vss	50	CKE0	80	Vss	110	Vss
21	DQ16	51	Vdd	81	DQ32	111	DQS7#
22	DQ17	52	BA2	82	DQ33	112	DQS7
23	Vss	53	NC	83	Vss	113	Vss
24	DQS2#	54	Vdd	84	DQS4#	114	DQ58
25	DQS2	55	A11	85	DQS4	115	DQ59
26	Vss	56	A7	86	Vss	116	Vss
27	DQ18	57	Vdd	87	DQ34	117	SA0
28	DQ19	58	A5	88	DQ35	118	SCL
29	Vss	59	A4	89	Vss	119	SA2
30	DQ24	60	Vdd	90	DQ40	120	Vtt

240-Pin DDR3 ECC DIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	Vss	151	Vss	181	A1	211	Vss
122	DQ4	152	DM3	182	Vdd	212	DM5
123	DQ5	153	NC	183	Vdd	213	NC
124	Vss	154	Vss	184	CK0	214	Vss
125	DM0	155	DQ30	185	CK0#	215	DQ46
126	NC	156	DQ31	186	Vdd	216	DQ47
127	Vss	157	Vss	187	EVENT#	217	VSS
128	DQ6	158	CB4	188	A0	218	DQ52
129	DQ7	159	CB5	189	Vdd	219	DQ53
130	Vss	160	Vss	190	BA1	220	Vss
131	DQ12	161	DM8	191	Vdd	221	DM6
132	DQ13	162	NC	192	RAS#	222	NC
133	Vss	163	Vss	193	S0#	223	Vss
134	DM1	164	CB6	194	Vdd	224	DQ54
135	NC	165	CB7	195	ODT0	225	DQ55
136	Vss	166	Vss	196	A13	226	Vss
137	DQ14	167	NC	197	Vdd	227	DQ60
138	DQ15	168	RESET#	198	NC	228	DQ61
139	Vss	169	CKE1	199	Vss	229	Vss
140	DQ20	170	Vdd	200	DQ36	230	DM7
141	DQ21	171	A15	201	DQ37	231	NC
142	Vss	172	A14	202	Vss	232	Vss
143	DM2	173	Vdd	203	DM4	233	DQ62
144	NC	174	A12	204	NC	234	DQ63
145	Vss	175	A9	205	Vss	235	Vss
146	DQ22	176	Vdd	206	DQ38	236	Vddspd
147	DQ23	177	A8	207	DQ39	237	SA1
148	Vss	178	A6	208	Vss	238	SDA
149	DQ28	179	Vdd	209	DQ44	239	Vss
150	DQ29	180	A3	210	DQ45	240	Vtt

Pin Description

Symbol	Type	Description
A[15:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as “BL on-the-fly” during CAS commands. The address inputs also provide the op-code during the mode register command set. A[13:0] address the 1Gb DDR3 devices. A[15:14] are needed to calculate parity on the command/address bus.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command. BA[2:0] are used as part of the parity calculation.
CK0, CK0#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE[1:0]	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DM[8:0] (TDQS[17:9], TDQS#[17:9])	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of the DQS. Although the DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins. When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance, otherwise the TDQS# pins are no function.
ODT[1:0]	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DRAM. When enabled in normal operation, ODT is applied only to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for the address, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW CMOS input referenced to Vss. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × Vdd and DC LOW ≤ 0.2 × Vdd.
S#[1:0]	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Serial address inputs:** These pins are used to configure the temperature sensor/SPD EEPROM address range on the I2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** SCL is used to synchronize communication to and from the temperature sensor/SPD EEPROM.
CB[7:0]	I/O	**Check bits:** Data used for ECC.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[8:0], DQS#[8:0]	I/O	**Data strobe:** DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. DQS# is used only when the differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the module on the I2C bus.
Err_Out#	Output (open-drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open-drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
Vdd	Supply	**Power supply:** 1.5V ±0.075V. The component Vdd and Vddq are connected to the module Vdd.
Vddspd	Supply	**Temperature sensor/SPD EEPROM power supply:** +3.0V to +3.6V.
Vrefca	Supply	**Reference voltage:** Control, command, and address (Vdd/2).
Vrefdq	Supply	**Reference voltage:** DQ, DM (Vdd/2).
Vss	Supply	Ground.
Vtt	Supply	**Termination voltage:** Used for control, command, and address (Vdd/2).
NC	–	**No connect:** These pins are not connected on the module.
NU	–	**Not used:** These pins are not used in specific module configuration/operations.

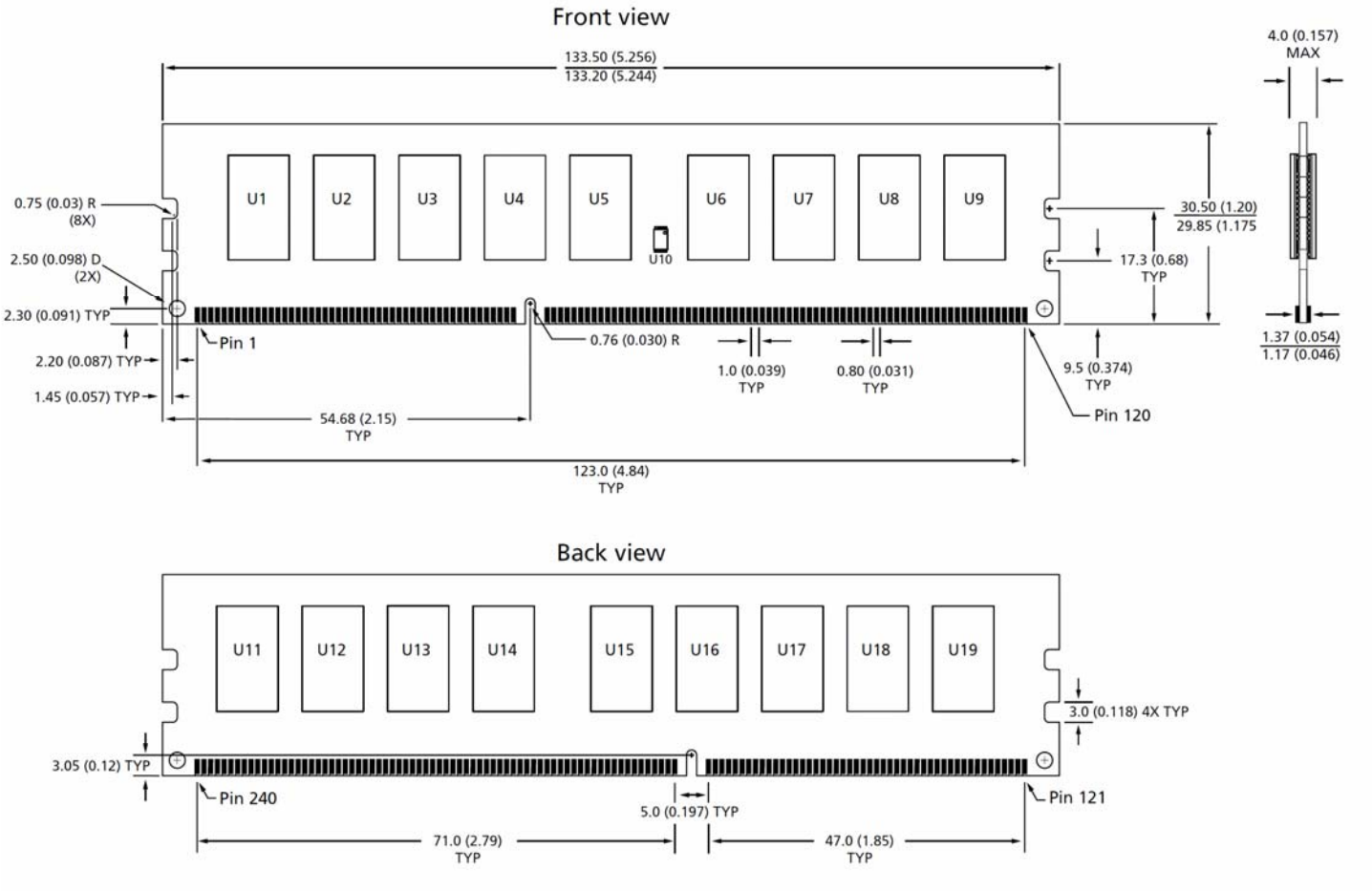
Simplified Mechanical Drawing(x8 1Rank)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

Simplified Mechanical Drawing(x8 2Ranks)



Note 1: All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note 2: The dimensional diagram is for reference only.